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Application Note

A PHASE-LOCKED LOOP TUNING SYSTEM FOR TELEVISION

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This note describes a frequency domain tuning system which utilizes direct digital countdown of the varactor tuner's local oscillator to obtain the proper local oscillator frequency for the channel number selected. The system features direct channel access with equal ease of tuning and an exact channel readout for all VHF and UHF channels.

MOTOROLA *Semiconductor Products Inc.*

A PHASE-LOCKED LOOP TUNING SYSTEM FOR TELEVISION

INTRODUCTION

This application note shows that a completely digital, direct divide-down phase-locked loop tuning system for television is possible. This frequency domain varactor tuning system eliminates the factory and customer adjustments that must be made on the tuning pots and channel readouts associated with analog tuning systems. The constant problems of obtaining the proper varactor tuning voltages and the needed variable range automatic fine tuning are eliminated.

The system features direct channel access with equal ease of tuning for all VHF and UHF channels. The exact channel number that was entered into the system and its validity are displayed on the two seven-segment readouts. The basic block diagram of the PLL tuning system is shown in Figure 1.

Since the basic theory of PLL systems has been widely available in recent times, no overall system discussion will be undertaken. Instead, each block shown in Figure 1 will be described in detail, and any interacting considerations covered as required.

CUSTOMER INTERFACE

The customer interface circuit is shown in Figure 2. This circuit gives the user a means to enter a channel number, and gives the system a way to tell the user what channel or portion of a channel number has been entered, and if that number is valid.

A ten-button keyboard was chosen as the means to enter the channel number. The user must sequentially press two keys to make a complete entry for any channel. The first key pressed will load the tens section of the data latch, and the second key pressed will load the units section. The keyboard buttons are decoded into binary coded decimal by eleven diodes, and the information is loaded into each section of the MC8308P dual data latch by bringing the enable input of the appropriate section low when a button is pressed. This is accomplished by the data input steering section. Four diodes form an OR gate to generate a positive going edge on the input of the MC8601P one-shot whenever there is any activity on the keyboard. The one-shot is used to clean the leading edge noise caused by the keyboard switch contact bounce. The Q output of the one-shot is connected to one-half of the MC7479P dual flip-flop. Assume that the user wants to enter channel number five. The zero key must first be pressed; this causes the input of the one-shot to go high. The one-shot will trigger and cause the $\overline{Q}$ output of the flip-flop to go low. This will in turn trigger one-half of the MC8602P dual one-shot and the $\overline{Q}_A$ output will go low for 1.5 ms and cause the tens section of the data latch to load the zero present at the inputs. The tens portion of the desired channel number is now entered and displayed on the readout. The sound and picture mute line will go high and the units section of the channel readout will be blanked telling the user that only half of the channel number has been entered and that the system is waiting for units data. The user will now press

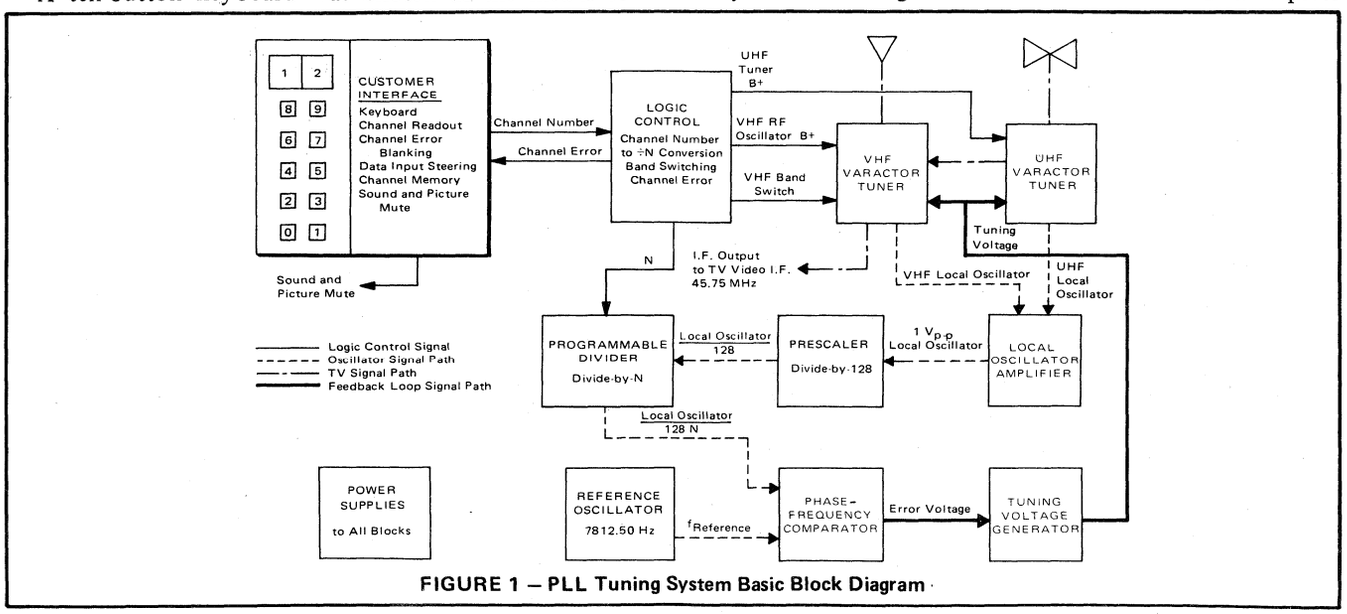

FIGURE 1 – PLL Tuning System Basic Block Diagram

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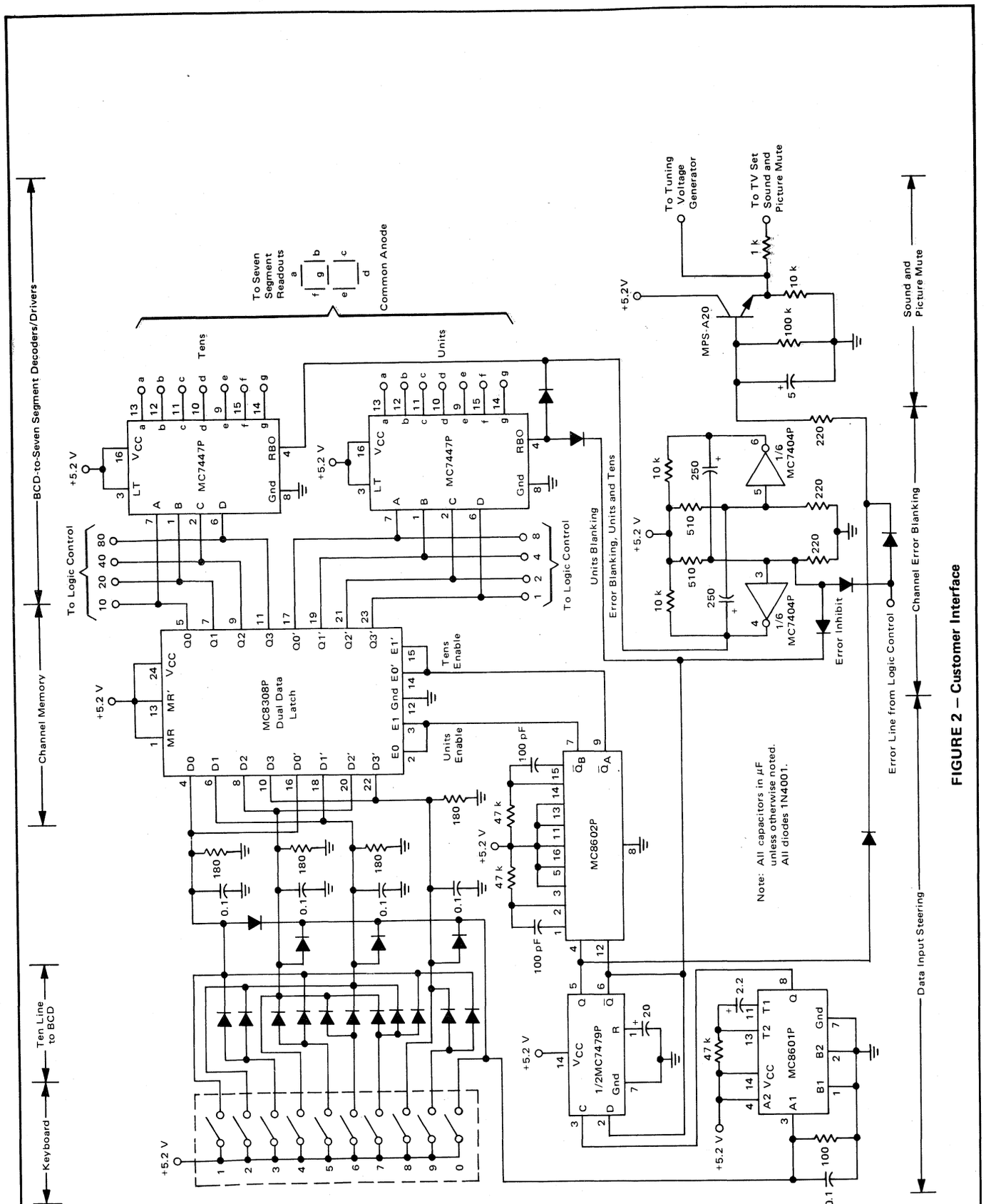

FIGURE 2 – Customer Interface

key number five, causing the input of the first one-shot to go high again. When this event takes place, the $\overline{Q}$ output of the flip-flop will return to its normally high state, and the Q output will go low, causing the second half of the MC8602P to trigger. At this instant, the units section of the channel readout will unblank. The $\overline{Q}_B$ output of the one-shot will go low for 1.5 ms and cause the units section of the data latch to load the BCD five present at the inputs.

The user has now completed the channel entry and if the number entered was a valid TV channel number, the sound and picture mute line will return to a low state. If not, the mute line will remain high and the channel readout will flash the invalid number at a two-hertz rate. This will occur until a tens digit entry is made. The channel number validity is determined by the logic control section described later. The outputs of the dual data latch are fed to the logic control section and to the inputs of the two MC7447P BCD-to-seven segment decoder/display drivers. If the 5.2 V supply is connected so that the dual data latch is powered while the set is off, the last channel number entered will be present when the set is turned on again.

LOGIC CONTROL

The logic control circuit shown in Figure 3 performs three main functions. (1) It converts the two-digit channel number entered into a three-digit divide-by-N number needed by the programmable divider. (2) It determines which band the desired channel is located within, turns on the appropriate tuner, and applies the proper bias for the bandswitching on the VHF tuner. (3) It determines if the channel number entered is valid; if it is not, an error signal is generated which is fed to the customer interface circuit to flash the channel readouts, mute the sound, and blank the picture.

The central element of the logic control is the 100-word by 15-bit memory which is composed of four 64-word by 8-bit programmable read-only memories, MCM5004L. The PROMs are wired in parallel to increase the number of bits per word, and wired in series to increase the number of words. The number that is programmed into the PROMs is equal to the tuner local oscillator frequency in megahertz for the desired channel. For example, if the user desires the receiver to be tuned to channel 10, a 10 is entered at the keyboard and appears in BCD form at the inputs of the logic control circuit. The output of the logic control circuit will contain the number 239 in BCD form, which is fed to the programmable divider. The counter will now divide by 239. A chart of channel number versus tuner local oscillator frequency is shown in Figure 4, along with the proper band switch, tuner B+, and error data. After examining the chart, it becomes apparent that the largest common denominator for all 82 tuner

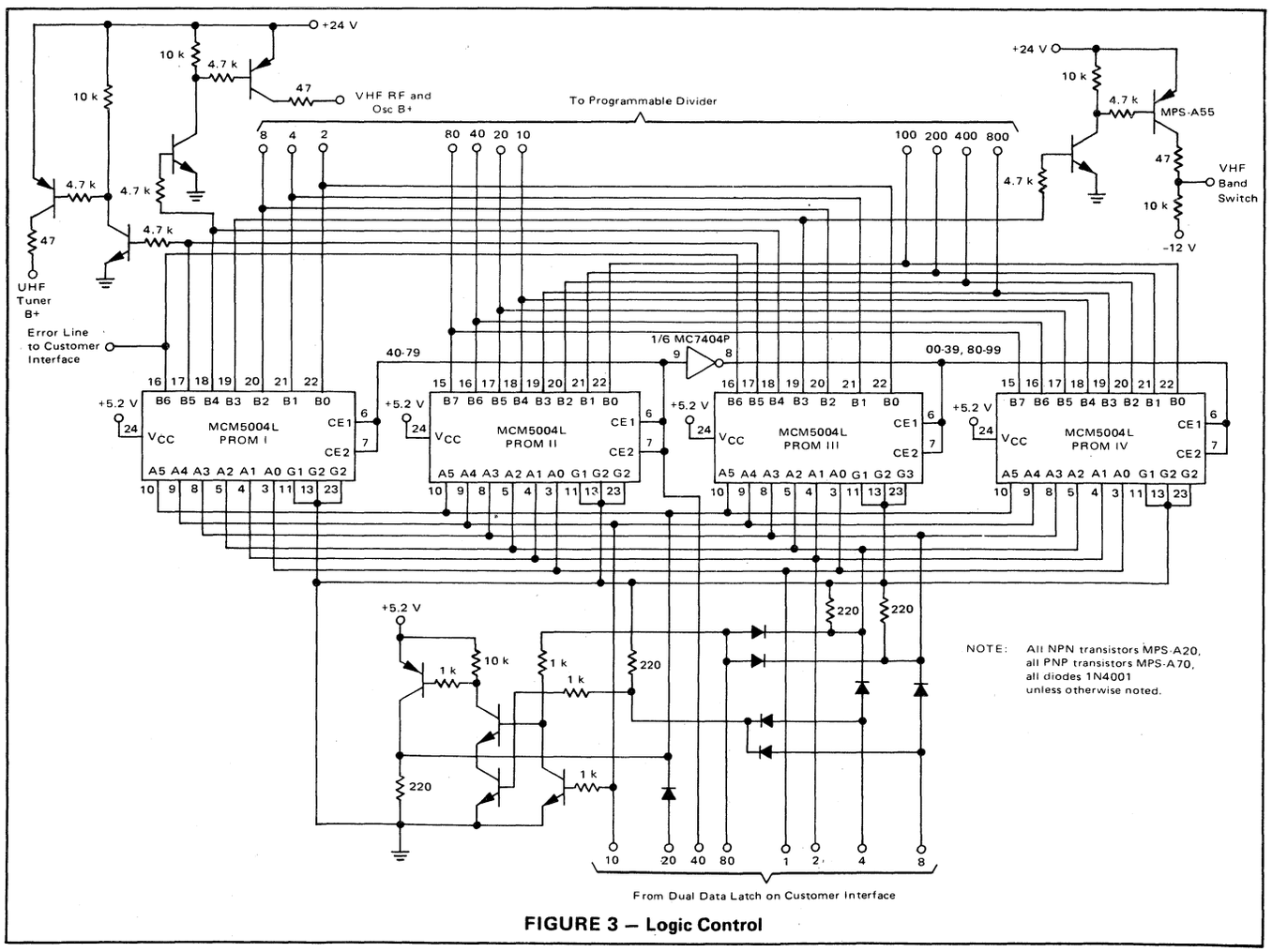

FIGURE 3 – Logic Control

Channel Number	Picture Carrier Frequency (MHz)	Tuner Oscillator Frequency (MHz)	Programmable Divider Input											UHF Band-Switch	VHF RF and Osc	UHF B+	Error
			Hundreds				Tens				Units						
			800	400	200	100	80	40	20	10	8	4	2				
0	–	–	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
1	–	–	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
2	55.25	101	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
3	61.25	107	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0
4	67.25	113	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0
5	77.25	123	0	0	0	1	0	0	1	0	0	0	1	0	1	0	0
6	83.25	129	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0
7	175.25	221	0	0	1	0	0	0	1	0	0	0	0	1	1	0	0
8	181.25	227	0	0	1	0	0	0	1	0	0	1	1	1	1	0	0
9	187.25	233	0	0	1	0	0	0	1	1	0	0	1	1	1	0	0
10	193.25	239	0	0	1	0	0	0	1	1	1	0	0	1	1	0	0
11	199.25	245	0	0	1	0	0	1	0	0	0	1	0	1	1	0	0
12	205.25	251	0	0	1	0	0	1	0	1	0	0	0	1	1	0	0
13	211.25	257	0	0	1	0	0	1	0	1	0	1	1	1	1	0	0
14	471.25	517	0	1	0	1	0	0	0	1	0	1	1	1	0	1	0
15	477.25	523	0	1	0	1	0	0	1	0	0	0	1	1	0	1	0
16	483.25	529	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0
17	489.25	535	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0
18	495.25	541	0	1	0	1	0	1	0	0	0	0	0	1	0	1	0
19	501.25	547	0	1	0	1	0	1	0	0	0	1	1	1	0	1	0
20	507.25	553	0	1	0	1	0	1	0	1	0	0	1	1	0	1	0
21	513.25	559	0	1	0	1	0	1	0	1	1	0	0	1	0	1	0
22	519.25	565	0	1	0	1	0	1	1	0	0	1	0	1	0	1	0
23	525.25	571	0	1	0	1	0	1	1	1	0	0	0	1	0	1	0
24	531.25	577	0	1	0	1	0	1	1	1	0	1	1	1	0	1	0
25	537.25	583	0	1	0	1	1	0	0	0	0	0	1	1	0	1	0
26	543.25	589	0	1	0	1	1	0	0	0	1	0	0	1	0	1	0
27	549.25	595	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
28	555.25	601	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0
29	561.25	607	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
30	567.25	613	0	1	1	0	0	0	0	1	0	0	1	1	0	1	0
31	573.25	619	0	1	1	0	0	0	0	1	1	0	0	1	0	1	0
32	579.25	625	0	1	1	0	0	0	1	0	0	1	0	1	0	1	0
33	585.25	631	0	1	1	0	0	0	1	1	0	0	0	1	0	1	0
34	591.25	637	0	1	1	0	0	0	1	1	0	1	1	1	0	1	0
35	597.25	643	0	1	1	0	0	1	0	0	0	0	1	1	0	1	0
36	603.25	649	0	1	1	0	0	1	0	0	1	0	0	1	0	1	0
37	609.25	655	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0
38	615.25	661	0	1	1	0	0	1	1	0	0	0	0	1	0	1	0
39	621.25	667	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0
40	627.25	673	0	1	1	0	0	1	1	1	0	0	1	1	0	1	0
41	633.25	679	0	1	1	0	0	1	1	1	1	0	0	1	0	1	0
42	639.25	685	0	1	1	0	1	0	0	0	0	1	0	1	0	1	0
43	645.25	691	0	1	1	0	1	0	0	1	0	0	0	1	0	1	0
44	651.25	697	0	1	1	0	1	0	0	1	0	1	1	1	0	1	0
45	657.25	703	0	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	663.25	709	0	1	1	1	0	0	0	0	1	0	0	1	0	1	0
47	669.25	715	0	1	1	1	0	0	0	1	0	1	0	1	0	1	0
48	675.25	721	0	1	1	1	0	0	1	0	0	0	0	1	0	1	0
49	681.25	727	0	1	1	1	0	0	1	0	0	1	1	1	0	1	0
50	687.25	733	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0
51	693.25	739	0	1	1	1	0	0	1	1	1	0	0	1	0	1	0
52	699.25	745	0	1	1	1	0	1	0	0	0	1	0	1	0	1	0
53	705.25	751	0	1	1	1	0	1	0	1	0	0	0	1	0	1	0
54	711.25	757	0	1	1	1	0	1	0	1	0	1	1	1	0	1	0
55	717.25	763	0	1	1	1	0	1	1	0	0	0	1	1	0	1	0
56	723.25	769	0	1	1	1	0	1	1	0	1	0	0	1	0	1	0
57	729.25	775	0	1	1	1	0	1	1	1	0	1	0	1	0	1	0
58	735.25	781	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
59	741.25	787	0	1	1	1	1	0	0	0	0	1	1	1	0	1	0
60	747.25	793	0	1	1	1	1	0	0	1	0	0	1	1	0	1	0
61	753.25	799	0	1	1	1	1	0	0	1	1	0	0	1	0	1	0
62	759.25	805	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0
63	765.25	811	1	0	0	0	0	0	0	1	0	0	0	1	0	1	0
64	771.25	817	1	0	0	0	0	0	0	1	0	1	1	1	0	1	0
65	777.25	823	1	0	0	0	0	0	1	0	0	0	1	1	0	1	0
66	783.25	829	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0
67	789.25	835	1	0	0	0	0	0	1	1	0	1	0	1	0	1	0
68	795.25	841	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0
69	801.25	847	1	0	0	0	0	1	0	0	0	1	1	1	0	1	0
70	807.25	853	1	0	0	0	0	1	0	1	0	0	1	1	0	1	0
71	813.25	859	1	0	0	0	0	1	0	1	1	0	0	1	0	1	0
72	819.25	865	1	0	0	0	0	1	1	0	0	1	0	1	0	1	0
73	825.25	871	1	0	0	0	0	1	1	1	0	0	0	1	0	1	0
74	831.25	877	1	0	0	0	0	1	1	1	0	1	1	1	0	1	0
75	837.25	883	1	0	0	0	1	0	0	0	0	0	1	1	0	1	0
76	843.25	889	1	0	0	0	1	0	0	0	1	0	0	1	0	1	0
77	849.25	895	1	0	0	0	1	0	0	1	0	1	0	1	0	1	0
78	855.25	901	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0
79	861.25	907	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0
80	867.25	913	1	0	0	1	0	0	0	1	0	0	1	1	0	1	0
81	873.25	919	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0
82	879.25	925	1	0	0	1	0	0	1	0	0	1	0	1	0	1	0
83	885.25	931	1	0	0	1	0	0	1	1	0	0	0	1	0	1	0
84-99	–	–	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1

X = Don't Care

FIGURE 4 – TV Tuner Address System, 100-Word x 15-Bit ROM

Word No.	PROM I To Control Line: –	Er	UHF	VHF	BSw	8	4	2	PROM II To Control Line: 80	40	20	10	800	400	200	100	Ch. No.
	Bit No. 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	0	1	0	1	1	1	0	1	1	0	40
1	0	0	1	0	1	1	0	0	0	1	1	1	0	1	1	0	41
2	0	0	1	0	1	0	1	0	1	0	0	0	0	1	1	0	42
3	0	0	1	0	1	0	0	0	1	0	0	1	0	1	1	0	43
4	0	0	1	0	1	0	1	1	1	0	0	1	0	1	1	0	44
5	0	0	1	0	1	0	0	1	0	0	0	0	0	1	1	1	45
6	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	46
7	0	0	1	0	1	0	1	0	0	0	0	1	0	1	1	1	47
8	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1	1	48
9	0	0	1	0	1	0	1	1	0	0	1	0	0	1	1	1	49
10																	
11																	
12																	
13																	
14																	
15																	
16	0	0	1	0	1	0	0	1	0	0	1	1	0	1	1	1	50
17	0	0	1	0	1	1	0	0	0	0	1	1	0	1	1	1	51
18	0	0	1	0	1	0	1	0	0	1	0	0	0	1	1	1	52
19	0	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	53
20	0	0	1	0	1	0	1	1	0	1	0	1	0	1	1	1	54
21	0	0	1	0	1	0	0	1	0	1	1	0	0	1	1	1	55
22	0	0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	56
23	0	0	1	0	1	0	1	0	0	1	1	1	0	1	1	1	57
24	0	0	1	0	1	0	0	0	1	0	0	0	0	1	1	1	58
25	0	0	1	0	1	0	1	1	1	0	0	0	0	1	1	1	59
26																	
27																	
28																	
29																	
30																	
31																	
32	0	0	1	0	1	0	0	1	1	0	0	1	0	1	1	1	60
33	0	0	1	0	1	1	0	0	1	0	0	1	0	1	1	1	61
34	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	62
35	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	0	63
36	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	64
37	0	0	1	0	1	0	0	1	0	0	1	0	1	0	0	0	65
38	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	66
39	0	0	1	0	1	0	1	0	0	0	1	1	1	0	0	0	67
40	0	0	1	0	1	0	0	0	0	1	0	0	1	0	0	0	68
41	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	69
42																	
43																	
44																	
45																	
46																	
47																	
48	0	0	1	0	1	0	0	1	0	1	0	1	1	0	0	0	70
49	0	0	1	0	1	1	0	0	0	1	0	1	1	0	0	0	71
50	0	0	1	0	1	0	1	0	0	1	1	0	1	0	0	0	72
51	0	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0	73
52	0	0	1	0	1	0	1	1	0	1	1	1	1	0	0	0	74
53	0	0	1	0	1	0	0	1	1	0	0	0	1	0	0	0	75
54	0	0	1	0	1	1	0	0	1	0	0	0	1	0	0	0	76
55	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0	0	77
56	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	78
57	0	0	1	0	1	0	1	1	0	0	0	0	1	0	0	1	79
58																	
59																	
60																	
61																	
62																	
63																	

Word No.	PROM III To Control Line: –	Er	UHF	VHF	BSw	8	4	2	PROM IV To Control Line: 80	40	20	10	800	400	200	100	Ch. No.
	Bit No. 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	2
3	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	1	3
4	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	4
5	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	5
6	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	6
7	0	0	0	1	1	0	0	0	0	0	1	0	0	0	1	0	7
8	0	0	0	1	1	0	1	1	0	0	1	0	0	0	1	0	8
9	0	0	0	1	1	0	0	1	0	0	1	1	0	0	1	0	9
10																	
11																	
12	0	0	1	0	1	0	0	1	0	0	0	1	1	0	0	1	80
13	0	0	1	0	1	1	0	0	0	0	0	1	1	0	0	1	81
14	0	0	1	0	1	0	1	0	0	0	1	0	1	0	0	1	82
15	0	0	1	0	1	0	0	0	0	0	1	1	1	0	0	1	83
16	0	0	0	1	1	1	0	0	0	0	1	1	0	0	1	0	10
17	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	11
18	0	0	0	1	1	0	0	0	0	1	0	1	0	0	1	0	12
19	0	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	13
20	0	0	1	0	1	0	1	1	0	0	0	1	0	1	0	1	14
21	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	1	15
22	0	0	1	0	1	1	0	0	0	0	1	0	0	1	0	1	16
23	0	0	1	0	1	0	1	0	0	0	1	1	0	1	0	1	17
24	0	0	1	0	1	0	0	0	0	1	0	0	0	1	0	1	18
25	0	0	1	0	1	0	1	1	0	1	0	0	0	1	0	1	19
26																	
27																	
28	0	1	1	0	1												90,94,98
29	0	1	1	0	1												91,95,99
30	0	1	1	0	1												92,96
31	0	1	1	0	1												93,97
32	0	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	20
33	0	0	1	0	1	1	0	0	0	1	0	1	0	1	0	1	21
34	0	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	22
35	0	0	1	0	1	1	0	0	0	1	1	1	0	1	0	1	23
36	0	0	1	0	1	0	1	1	0	1	1	1	0	1	0	1	24
37	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0	1	25
38	0	0	1	0	1	1	0	0	1	0	0	0	0	1	0	1	26
39	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	27
40	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	28
41	0	0	1	0	1	0	1	1	0	0	0	0	0	1	1	0	29
42																	
43																	
44	0	1	1	0	1	0	1	1	0	0	1	1	1	0	0	1	84,88
45	0	1	1	0	1	0	0	1	0	1	0	0	1	0	0	1	85,89
46	0	1	1	0	1	1	0	0	0	1	0	0	1	0	0	1	86
47	0	1	1	0	1	0	1	0	0	1	0	1	1	0	0	1	87
48	0	0	1	0	1	0	0	1	0	0	0	1	0	1	1	0	30
49	0	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	31
50	0	0	1	0	1	0	1	0	0	0	1	0	0	1	1	0	32
51	0	0	1	0	1	0	0	0	0	0	1	1	0	1	1	0	33
52	0	0	1	0	1	0	1	1	0	0	1	1	0	1	1	0	34
53	0	0	1	0	1	0	0	1	0	1	0	0	0	1	1	0	35
54	0	0	1	0	1	1	0	0	0	1	0	0	0	1	1	0	36
55	0	0	1	0	1	0	1	0	0	1	0	1	0	1	1	0	37
56	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	38
57	0	0	1	0	1	0	1	1	0	1	1	0	0	1	1	0	39
58																	
59																	
60																	
61																	
62																	
63																	

FIGURE 5 – PROM Program

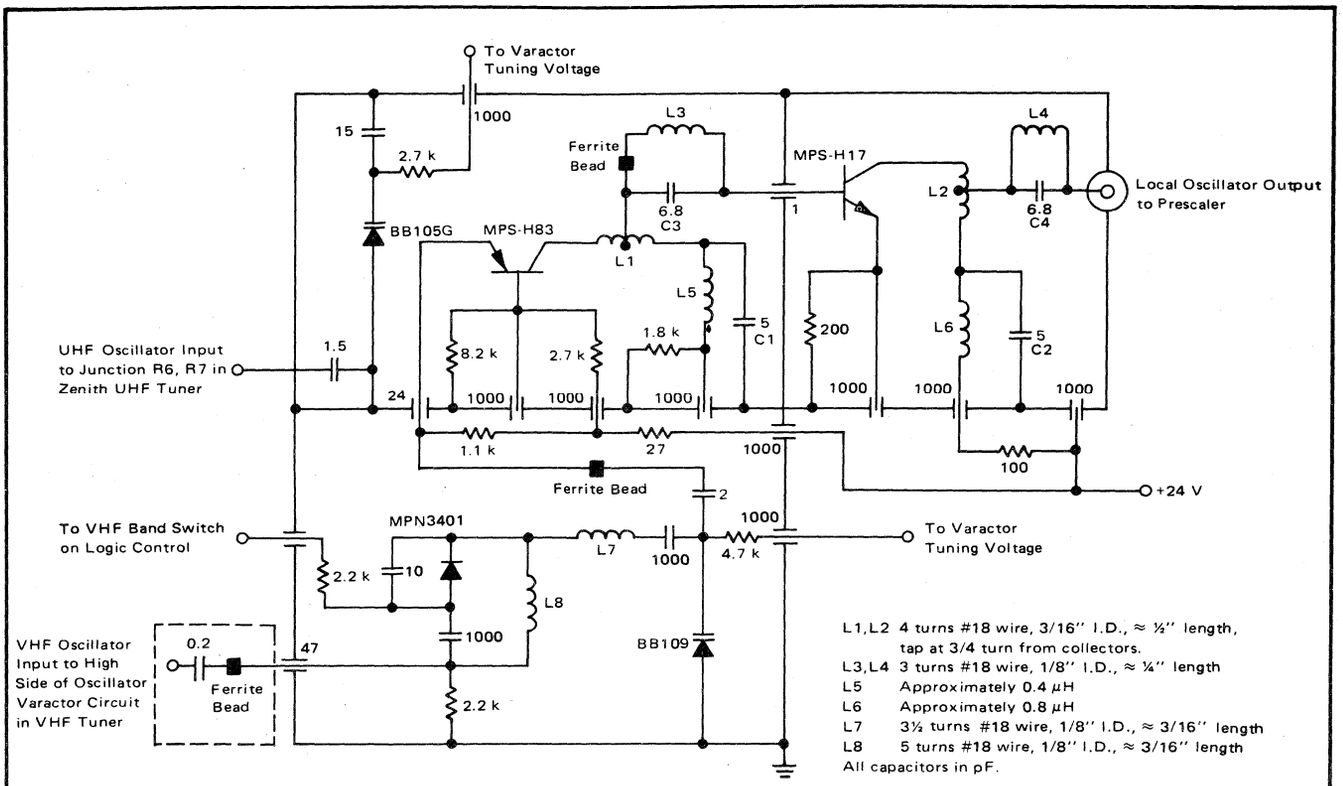

FIGURE 6 –Local Oscillator Amplifier

oscillator frequencies is 1 MHz. Therefore, the system design must be capable of stepping in 1-MHz increments from 101 to 931 MHz to establish a true on-station lock.

Since the PROMs are wired to expand the word bit length and the number of words, each of the four units has a different program. Figure 5 shows the program for each word bit for the four units. Refer to reference 1 for the programming information.

LOCAL OSCILLATOR AMPLIFIER

The local oscillator amplifier shown in Figure 6 was constructed in a small printed circuit board box mounted on the side of the UHF tuner. The VHF and UHF input sections are designed to track with the tuners' local oscillators in order to keep the harmonic outputs of the local oscillator greater than 30 dB down at the amplifier output. The minimum signal output across the VHF and UHF bands is 1 volt (p-p) across 50 ohms. A unique feature of this amplifier is that the VHF and UHF local oscillator inputs are separate and do not have to be switched. Elements L3, C3 and L4, C4 are parallel tuned for 380 MHz while elements L1, C1 and L2, C2 are both series tuned for 380 MHz. The output response of the amplifier, not including the tuned input circuits, is shown in Figure 7.

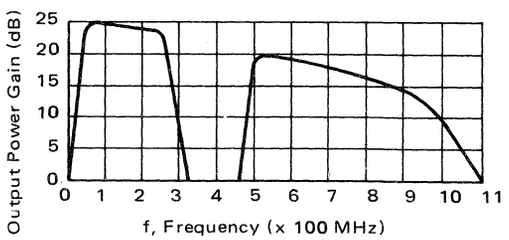

FIGURE 7 – Amplifier Output Response

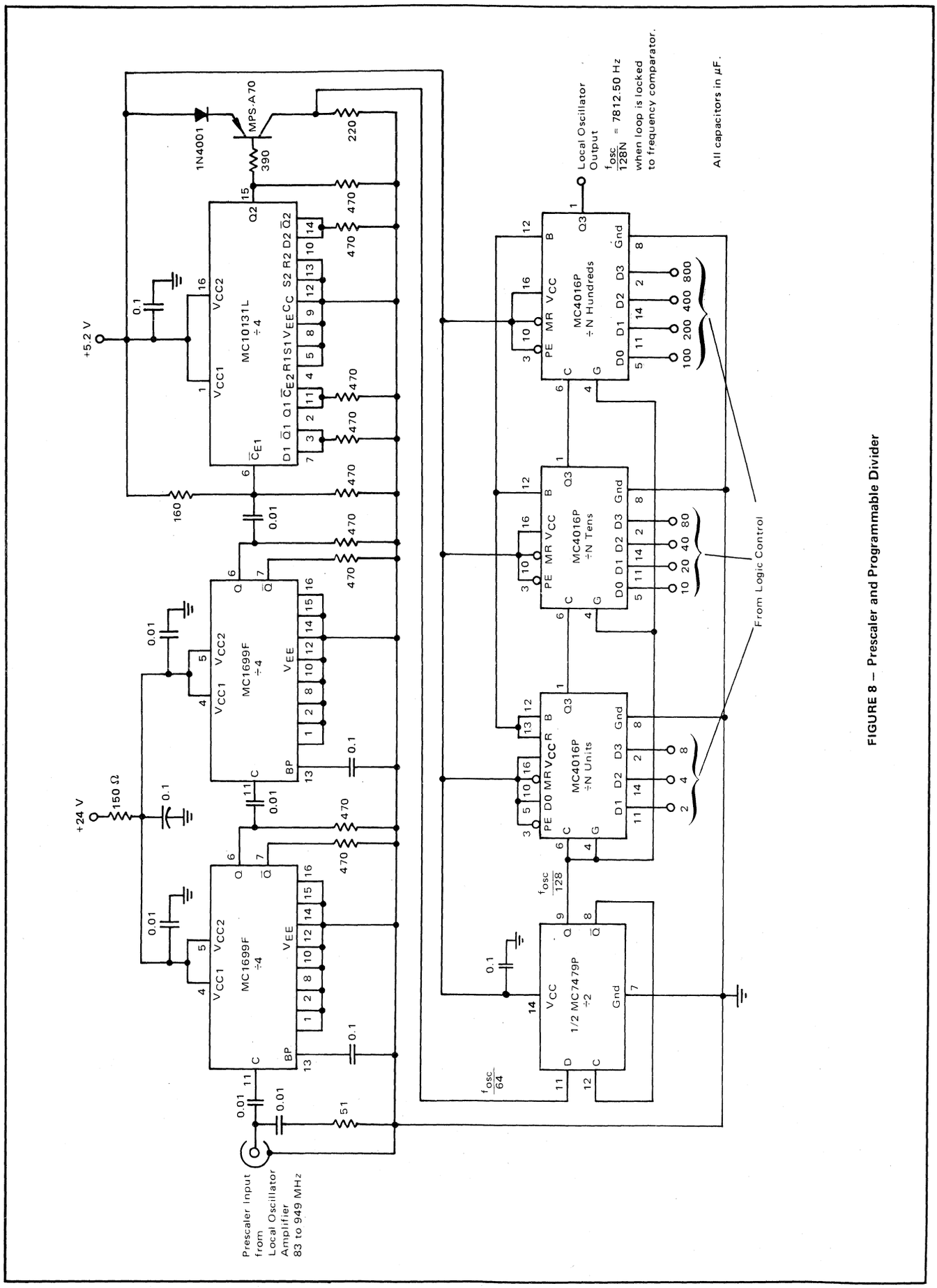

FIGURE 8 – Prescaler and Programmable Divider

PRESCALER AND PROGRAMMABLE DIVIDER

The circuit diagram of the prescaler and programmable divider is shown in Figure 8. The two MC1699F's and the MC10131L are MECL high-speed non-saturating logic and are cascaded to form a divide-by-64. The MC1699F is capable of dividing by 4 in excess of one gigahertz. An MPS-A70 transistor and a diode are used to translate from MECL to MTTL levels. One half of the MC7479P is used as a divide-by-2 which gives the prescaler section a total divisor of 128. The number 128 was chosen so that for channel 83 plus 18 MHz overshoot, a maximum of 7.414 MHz would be present at the input of the first programmable divider. This is well within the maximum toggle frequency capability of the MC4016P. Since the channel spacing capability of the system is 1 MHz and the input is prescaled by 128, then the reference frequency must be equal to 1 MHz/128 which is 7812.50 Hz.

The prescaler portion of the circuit was hand wired on a double-sided copper-clad board. The MECL integrated circuit packages were mounted on 1/2-inch centers with Dow Corning DC340 grease between the package and the copper-clad board. The lead lengths of the MECL integrated circuits and their associated components were kept to less than 1/32 of an inch. If the component lead lengths are excessive, the dividers may not toggle at some frequency within the band required, or they may oscillate when the input level drops too low to toggle the device. The first MC1699F requires 800 mV(p-p) to toggle it across the band, which is easily within the capability of the local oscillator amplifier.

PHASE-LOCKED LOOP SECTION

The circuit diagram of the reference oscillator, phase frequency comparator, and varactor voltage generator is shown in Figure 9. This section compares the prescaled and divided tuner oscillator frequency to the scaled reference oscillator frequency and generates a varactor tuning voltage in a corrective direction to obtain a frequency match. This system has a maximum tuning error at channel 83 of ±30 kHz because the reference crystal oscillator circuit is capable of less than ±0.0032% error.

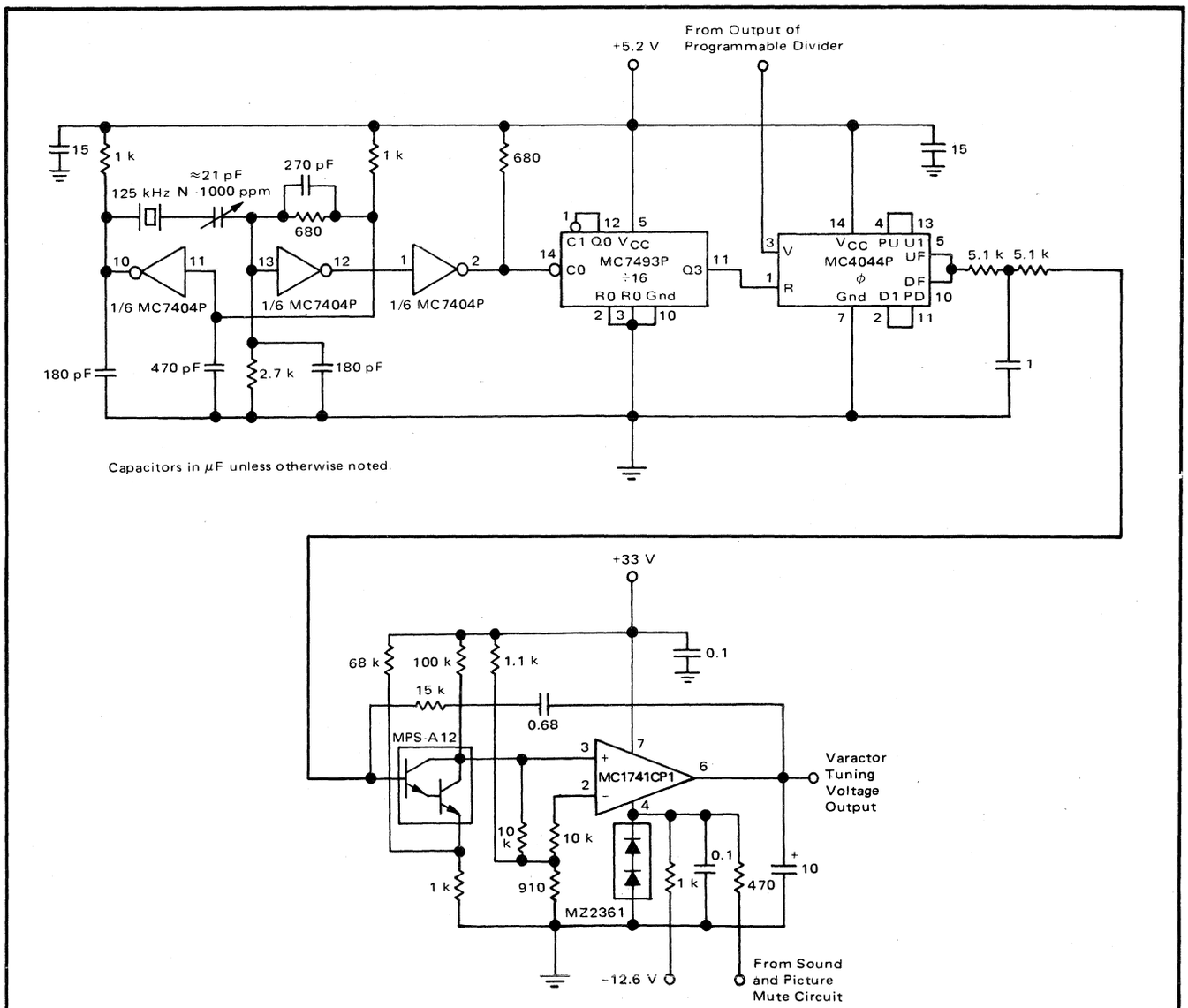

FIGURE 9 – Reference Oscillator, Phase-Frequency Comparator, and Varactor Voltage Generator

Two inverters are cross-coupled with a 125-kHz crystal to make the reference oscillator. A third inverter is used as a buffer to drive the MC7493P divide-by-16 to yield a reference frequency of 7812.5 Hz. This is fed into the reference input of the MC4044P phase-frequency comparator. The variable input is driven by the programmable divider. The charge pump output of the MC4044P is filtered and connected to the base of an MPS-A12 darlington transistor. The base should be at 1.5 V when the system has established a lock condition. If the voltage is above or below this value, the lock-up time will not be the same when changing a constant number of channels in either direction within any given band. The collector of the MPS-A12 is connected to the non-inverting input of the MC1741CP1 operational amplifier. The inverting input is biased at 15 V so that the op-amp output is capable of 0.75 to 31 V swing with +33 and -1.2 V power supplies. The 470 ohm resistor is connected from the -1.2 V supply to the sound and picture mute line. This prevents the varactor tuning voltage from going below 1.5 V when an incomplete or invalid channel entry is made. If an invalid channel entry of 00 or 01 is made and the 470 ohm resistor was disconnected, the phase-frequency detector will force the varactor tuning voltage low enough to cause the VHF and UHF tuner local oscillators to drop out. This will cause the tuning system to lock out when a valid entry is made, because the oscillators will "squeg" as they come on, when the varactor tuning voltage is brought above the drop-out level.

With the charge pump filter and feedback network values shown, the lock-up time is 300 ms from channels 14 to 83 and 83 to 14. This looks instantaneous to the user. The noise modulation on the varactor tuning voltage line is less than 1.7 mV(p-p) on channel 14, where the UHF tuner local oscillator has the greatest sensitivity.

POWER SUPPLIES

The power supplies shown in Figure 10 were constructed to generate the voltages needed to operate the tuning system and tuners for display purposes. These supplies would normally be part of the television receiver.

CONCLUSION

The system described uses a total semiconductor count of 20 integrated circuits, 15 transistors, and 31 diodes, not including the devices used in the power supplies. These devices are standard Motorola off-the-shelf building blocks. This system approach can be made more appealing by the use of custom integrated circuits which would be specifically designed for this application. With the use of present day technology, the tuning system could consist of 4 to 6 integrated circuits, 2 transistors, and 4 diodes. The variable

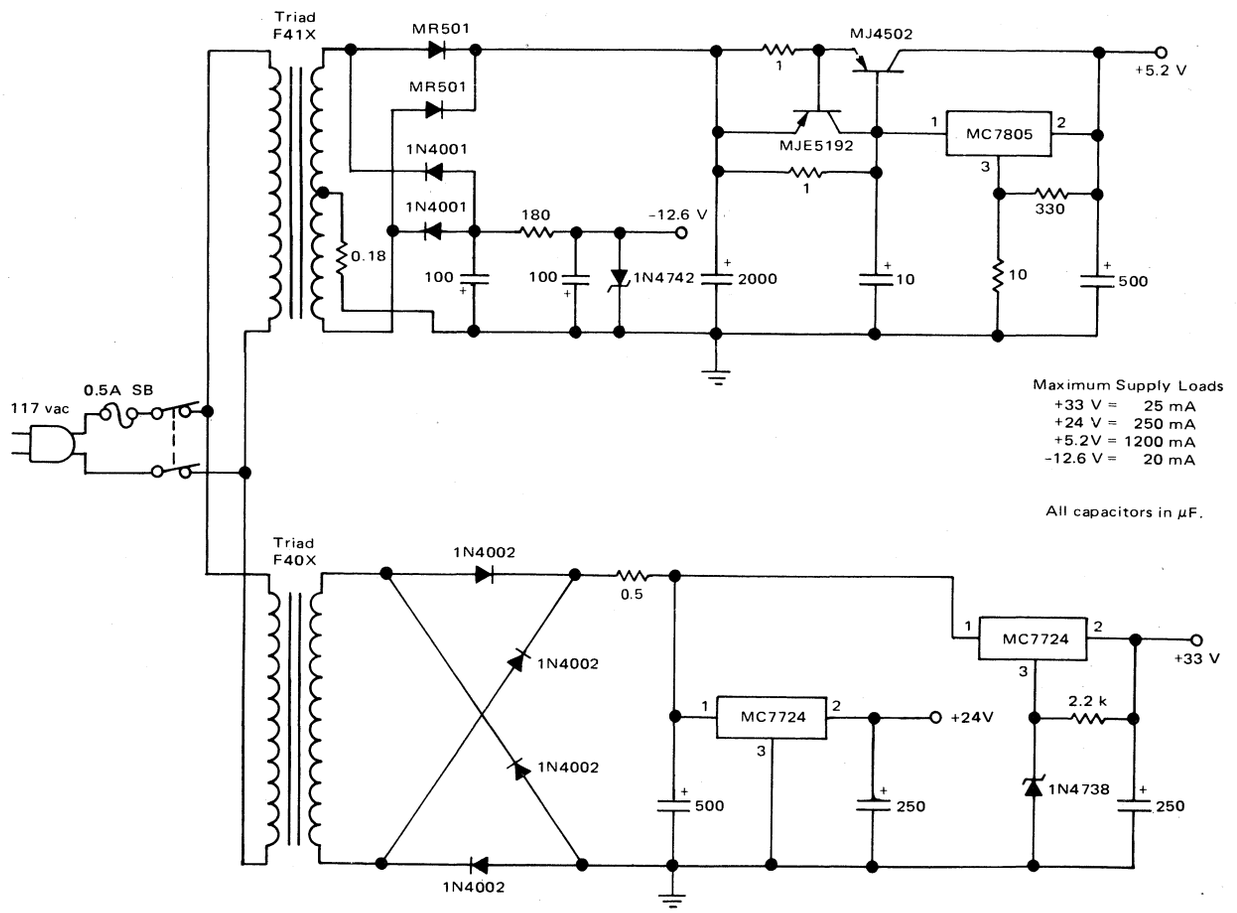

FIGURE 10 – Power Supplies

number of integrated circuits is dependent upon system partitioning.

It is hoped that this application note will stimulate more customer interest in the design of phase-locked loop tuning systems for television. Your suggestions and requirements will help us design and develop the custom integrated circuits needed for this type of approach.

The tuning system was connected to a Sony KV1201 color television. Figures 11 and 12 show the completed system.

REFERENCES

1. Prioste, Jerry E.: Programming the MCM5003/5004 Programmable Read Only Memories, Application Note AN-550, Motorola Semiconductor Products Inc.
2. Phase-Locked Loop Systems Data Book, Motorola Semiconductor Products Inc.

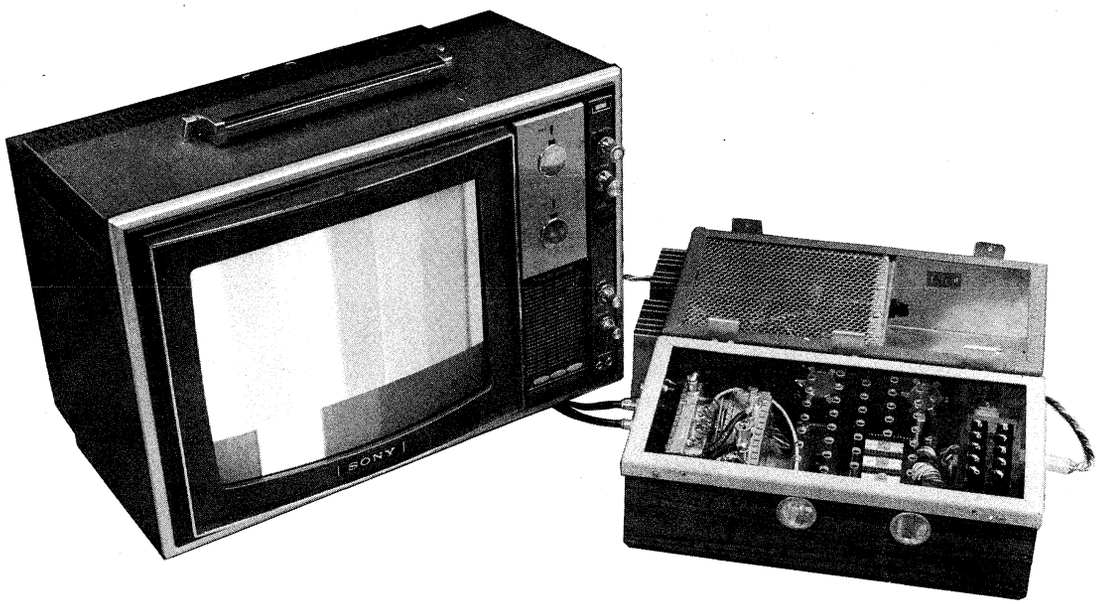

FIGURE 11

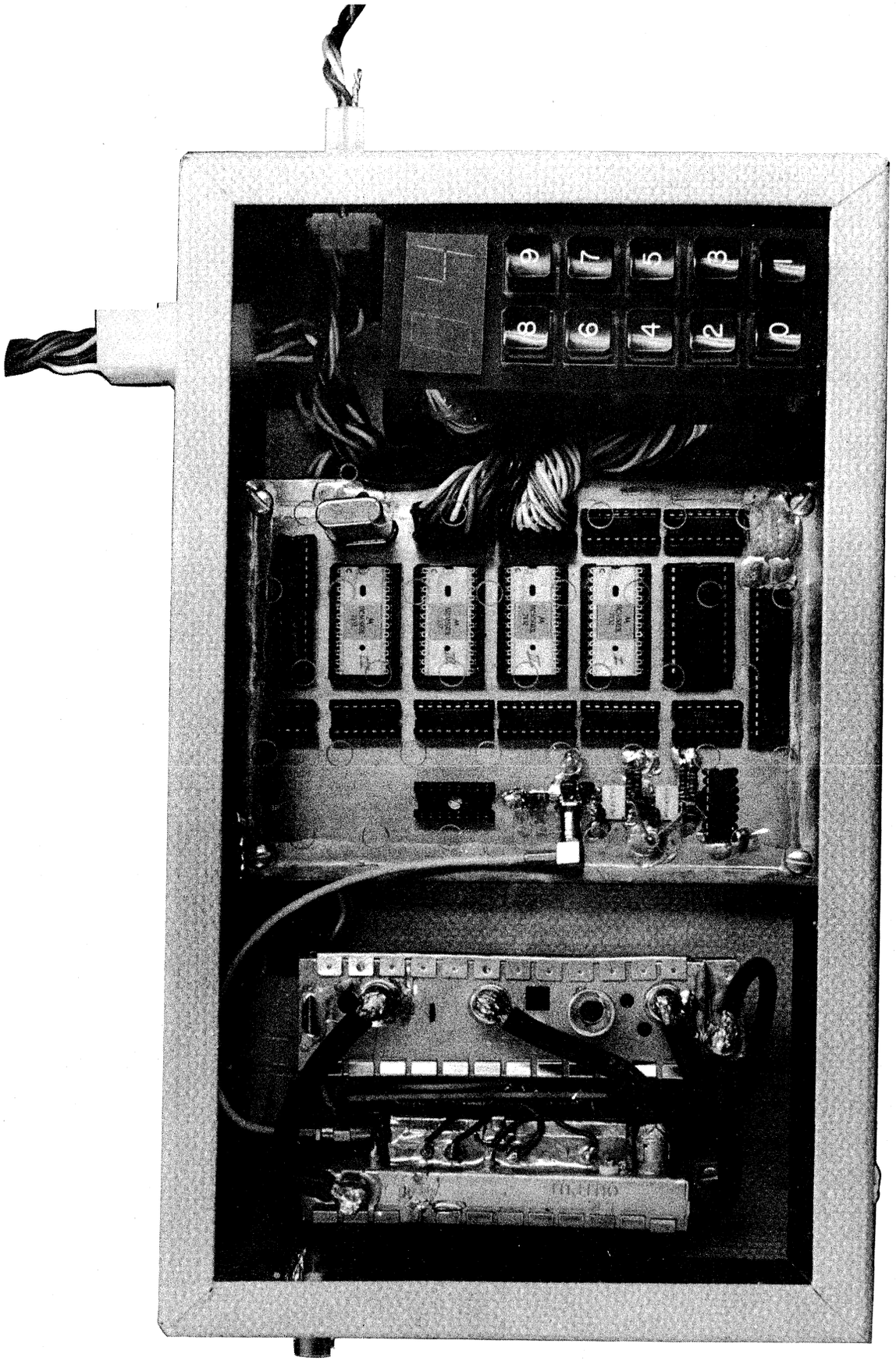

FIGURE 12